

Claims

1. A method for fabricating an antifuse structure (100) integrated with a semiconductor device, the method comprising the steps of:
 - forming a region of semiconducting material (11) overlying an insulator (3) disposed on a substrate (10);
 - performing an etching process to expose a plurality of corners (111-114) in the semiconducting material;
 - forming a plurality of elongated tips (111t, 112t, 113t, 114t) of the semiconducting material at the respective corners;
 - forming an oxide layer (51) on the semiconducting material and overlying the corners, the oxide layer having a nominal thickness and a reduced thickness at the corners less than the nominal thickness; and
 - forming a layer of conducting material (60) in contact with the oxide layer (51) at the corners,
 - thereby forming a plurality of possible breakdown paths at said corners, between the semiconducting material and the layer of conducting material through the oxide layer.
2. A method according to claim 1, characterized in that the step of forming the elongated tips comprises
 - oxidizing the exposed corners (111, 112, 113, 114) to form an oxide (31) thereon; and
 - removing the oxide (31) formed in said oxidizing step, prior to said step of forming an oxide layer (51).
3. A method according to claim 1 or claim 2, characterized in that the region of semiconducting material (11) is a fin formed in a FINFET process.

1 4. A method according to claim 1 or claim 2, characterized in that the region of
2 semiconducting material (211) is a gate region formed in a planar CMOS process.

1 5. A method according to claim 3 or claim 4, further comprising the step of doping the
2 region of semiconducting material (11, 211).

1 6. A method according to claim 2, characterized in that said oxidizing step is performed in
2 accordance with a low-temperature oxidation process.

1 7. A method according to any preceding claim, characterized in that the breakdown paths are
2 electrically in parallel.

1 8. A method according to any preceding claim, further comprising the step of applying a voltage
2 to the antifuse structure, thereby converting at least one of the breakdown paths to a conducting
3 path (103, 280) through the oxide layer (51, 251).

1 9. A method according to claim 8, characterized in that the voltage is applied in accordance
2 with a burn-in process for the device.

1 10. A method according to claim 8, characterized in that the device has a nominal voltage, and
2 the applied voltage is approximately 1.5 times the nominal voltage.

1 11. An antifuse structure (100) integrated with a semiconductor device, the structure
2 comprising:

3 a region of semiconducting material (11) overlying an insulator (3) disposed on a
4 substrate (10), the semiconducting material having a plurality of corners (111-114) with a
5 plurality of elongated tips (111t, 112t, 113t, 114t) of the semiconducting material at the
6 respective corners;

7 an oxide layer (51) on the semiconducting material and overlying the corners, the
8 oxide layer having a nominal thickness and a reduced thickness at the corners less than the

9 nominal thickness; and

10 a layer of conducting material (60) in contact with the oxide layer (51) at the corners,
11 characterized in that a plurality of possible breakdown paths are disposed at said
12 corners, between the semiconducting material and the layer of conducting material through the
13 reduced thickness of the oxide layer.

1 12. An antifuse structure according to claim 11, characterized in that the elongated tips are
2 formed by oxidation of the exposed corners (111, 112, 113, 114).

1 13. An antifuse structure according to claim 11 or claim 12, characterized in that the region of
2 semiconducting material (11) is a fin formed in a FINFET process.

1 14. An antifuse structure according to claim 11 or claim 12, characterized in that the region of
2 semiconducting material (211) is a gate region formed in a planar CMOS process.

1 15. An antifuse structure according to claim 13 or claim 14, characterized in that the region of
2 semiconducting material (11, 211) is a region of doped material.

1 16. An antifuse structure according to any preceding claim, characterized in that the breakdown
2 paths are electrically in parallel.

1 17. An antifuse structure according to any preceding claim, characterized in that at least one of
2 the breakdown paths is a conducting path (103, 280) through the oxide layer (51, 251) formed
3 by application of a voltage thereto.

1 18. An antifuse structure according to claim 17, characterized in that the applied voltage is a
2 burn-in voltage for the device.

1 19. An antifuse structure according to claim 18, characterized in that the device has a nominal
2 voltage, and the applied voltage is approximately 1.5 times the nominal voltage.